2.5D? 3D? What?
Overview of 3D Integrated Circuit Packaging and Test Challenges

Ira Feldman
November 11, 2011
Outline

- Why 2.5D & 3D ICs?
- Building stacks
  - TSV Processes
  - 2.5D & 3D stacks
  - Process & Test Flows
- Wafer Probe Solutions
- Key Organizations & Activities
- Future?
Disclaimer – This is the “new frontier” and things **will** change...
Package Proliferation

25+ Years of Semiconductor Packaging

ASE Begins

Leading edge CMOS node (approx): 0.25um, 0.18um, 0.13um, 90nm, 65nm, 40nm, 28nm


Sophistication & diversification increasing over time

“Backend to the Front Line” William Chen, ASE Group, SWTW 2011
Very low power & high density (small volume)
15x performance
90% less space
70% less power per bit*

* Micron – Hybrid Memory Cube
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“Stacking 1.0”

Wire Bonding

Sixteen 32Gb NAND Chips

Toshiba’s 64 GB Embedded NAND Flash Module
December 2009
TSV Processing

3D TSV via integration MAIN scenarios

<table>
<thead>
<tr>
<th>Step #1</th>
<th>Step #2</th>
<th>Step #3</th>
<th>Step #4</th>
<th>Step #5</th>
<th>Step #6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via First → Vias are made before CMOS</td>
<td>TSV Etch</td>
<td>TSV Fill</td>
<td>FEOL 1000°C</td>
<td>BEOL 450°C</td>
<td>Thinning + Backside prep</td>
</tr>
<tr>
<td>Via Middle → Vias are made between CMOS and BEOL</td>
<td>FEOL 1000°C</td>
<td>TSV Etch</td>
<td>TSV Fill</td>
<td>BEOL 450°C</td>
<td>Thinning + Backside prep</td>
</tr>
<tr>
<td>Via Last → Vias are made after BEOL</td>
<td>FEOL 1000°C</td>
<td>BEOL 450°C</td>
<td>Thinning</td>
<td>TSV Etch</td>
<td>TSV Fill</td>
</tr>
<tr>
<td>Via After Bonding → Vias are made after Bonding (C2W or W2W)</td>
<td>FEOL 1000°C + BEOL 450°C</td>
<td>Bonding</td>
<td>Thinning</td>
<td>TSV Etch</td>
<td>TSV Fill + Backside prep</td>
</tr>
</tbody>
</table>

Courtesy of Yole Developpement

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3D integration process options using TSV

- **TSV process flow**
  
  ![Diagram showing TSV process flow](image)

- **TSV interconnect methods**

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<tr>
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</thead>
<tbody>
<tr>
<td>Pros</td>
<td>Flexible Use of KGD</td>
<td>Flexible Use of KGD</td>
<td>High throughput</td>
</tr>
<tr>
<td>Cons</td>
<td>Handling, Bonding</td>
<td>Handling, Bonding</td>
<td>Same chip size, Yield</td>
</tr>
</tbody>
</table>

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“Panel Discussion: Advanced Packaging and 3D Technologies”, Kenichi Osada, Hitachi, 16th Asia and South Pacific Design Automation Conference (ASP-DAC) 2011
1. Introduction to TSV-Based 2.5D- and 3D-SICs

**Die Stacking**

**Endless Stacking Opportunities**
“Whatever your children can make using Lego bricks”

- **3D-SIC**

- **2½D-SIC**

- **2½D + 3D = 5½D-SIC**

“Wafer Probing on Fine-Pitch Micro-Bumps for 2.5D- and 3D-SICs”, Erik Jan Marinissen (IMEC), Peter Hanaway (Cascade Microtech), et. al.
Hybrid Memory Cube - Micron
Process Flow & Test Coverage

TODAY

- **Wafer Test**
  - Parametric
  - Fabricate
  - Fab Process Functionality
  - Partial to full speed

- **Final Test**
  - Packaged Part
  - Fab & Post Process Functionality
  - At full speed

- **Board Test**
  - Board/Module
  - PCA Process Functionality

- **System Test**
  - System
  - Integration Process Functionality
Known Good Die - Flow & Test Coverage

**TODAY**

**Wafer Test***
- Parametric
- Fabricate
  - Die (on wafer)
  - Fabricate
  - Func
  - Additional QA
- Fab Process
- Functionality

**Board Test**
- KGD
  - Place
  - Solder / Attach
- PCA Process
  - Functionality
- Board / Module

**System Test**
- Integrate
- System
- Integration Process
  - Functionality

* Predominant path to KGD is via wafer based testing. There are some solutions for die based socket testing such as Aehr Test's DiePak.

At full speed
Stacked Die – KGD (singulated)

KGD 1

Stack Test ???

Stack Process Functionality ???

At full speed???

KGD n

Die Stack

Board/Module

Integrate

System

Stack

Place Solder / Attach

Board Test

PCA Process Functionality

Integration Process Functionality

System Test

Siicon Valley Test Workshop 2011
Stacked Die – NKBD (wafers)

Wafers or reconstituted wafers of Not Known Bad Die:
• Thinned
• Partial to full speed tested
Stacked Die – Sub Stacks (wafers)

- Wafer 1
- Wafer n

**Memory Stack Test @ Memory Vendor**

**Full Stack Test @ Integrator ???**

CPU Wafer

Stack
“3D TSV Program Overview – Presented to GSA Oct 20, 2011” Sitaram Arkalgud, SEMATECH
Scan Testing

- Provide access and control to cores at all test steps
  - If proper infrastructure (P1838) & connectivity is present
  - Does not replace full access to all “pads” for KGD.

4. To-The-Point Please

**A Glimpse Of What We Are Thinking Of...**

- **Pre-Bond**
  - Die test

- **Mid/Post-Bond**
  - Die (re-)test
  - Interconnect test

- **Post-Packaging**
  - Die (re-)test
  - Interconnect (re-)test
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Mobile DRAM predecessor to Wide I/O

“A 1.2V 12.8GB/s 2Gb Mobile Wide-I/O DRAM with 4x128 I/Os Using TSV-Based Stacking” Jung-Sik Kim, et.al., Samsung Electronics, ISSCC 2011
Electroplated Micro-Bump Bonding

- Cylindrical bumps
  Side1: Cu (5 µm)
  Side2: CuSn (5 µm + 3.5 µm)

- Size (today)
  Diameter : 25 µm
  Pitch : 40 µm
  Scaling down...

Courtesy of Cascade Microtech & IMEC
FormFactor: NanoPierce Contact

Metal “NanoFiber” contact element

“A Low-Force MEMS Probe Solution For Fine-Pitch 3D-SIC Wafer Test”, Matthew W. Losey, et. al., 3D Test Workshop 2011

Probe beam: \( \sim 10 \, \mu m \times 80 \, \mu m \)
Cascade Microtech: Lithographically Printed

Fully-routed 6 x 50 array at 40 x 50 µm pitch
New space transformer technology

“Probing Strategies for Through-Silicon Stacking”,
Eric Strid, et. al, 3D Test Workshop 2011
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Developing Eco-system Standards and Clusters

3D IC Development & Test Standards

Memory (JC-42)
Wide IO (JC-42.6, JC-11)
Multi Chip Packaging (JC-63)
Qual & Rel (JC-14.3)

3D IC Enablement IP Standards

3D IC Packaging

3D Consortium 22 members

3DS-IC Wafer and Tool Standards
Bonded Wafer Pair (BWP) * Inspection and Metrology * Thin Wafer Carrier * Single Wafer in Stacked Process

37“3D IC Technology’s Promise for Communications and Storage ICs”, Brian D. Gerson, PMC-Sierra, GSA 4/28/11
Organizations & Programs

- **IEEE P1838** - Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits
  standards.ieee.org/develop/project/1838.html
- Semi [wiki.sematech.org/3D-Standards](http://wiki.sematech.org/3D-Standards)
- Sematech – 3D Program [www.sematech.org/research/3D](http://www.sematech.org/research/3D)
  - Unit Process, Module Development, Enablement Center
- Global Semiconductor Alliance – 3D-IC Working Group [www.gsaglobal.org/3dic](http://www.gsaglobal.org/3dic)
- JEDEC – Wide I/O [www.jedec.org](http://www.jedec.org)
- IMEC [www2.imec.be](http://www2.imec.be)
- Industrial Technology Research Institute (ITRI) [www.itri.org.tw](http://www.itri.org.tw)
Recent Conferences

- **GSA Memory Conference (Mar ’11)**

- **IEEE Semiconductor Wafer Test Workshop (June ’11 & ’12)**
  [www.swtest.org](http://www.swtest.org)

- **ATE Vision 2020 (w/Semicon West – Jul ’11)**
  [www.atevision.com](http://www.atevision.com)

- **Semicon Taiwan – SiP Global Summit 2011 (Sep ’11)**
  - 3D IC Test Forum [semicontaiwan.org/en/node/1566](http://semicontaiwan.org/en/node/1566)
  - 3D IC Technology Forum [semicontaiwan.org/en/node/1571](http://semicontaiwan.org/en/node/1571)

- **IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits (w/ITC – Sep ’11 / Nov ’12)**
  [3dtest.tttc-events.org](http://3dtest.tttc-events.org)

- **MEPTEC 2.5D, 3D and Beyond – Bringing 3D Integration to the Packaging Mainstream (Nov 9, 11)**
  [www.meptec.org](http://www.meptec.org)

- **MEPTEC-Semi KGD in an Era of Multi-Die Packaging and 3D Integration (Nov 10, 11)**
  [www.meptec.org](http://www.meptec.org)
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TBD - To Be Determined

- Yield
- Preferred Via Process
- Singulate dies before or after stacking
- Wafer probe and handling of die stacks on wafer or singulated stacks
- Business models – who is responsible for what
Future

- Hard work – getting it to work!
- Increased test complexity earlier in process
- Shrinks – especially micro-bumps and pitch
Thank You!

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Visit my blog
www.hightechbizdev.com
for additional resources.
Other References & Resources

- Hybrid Memory Cube Consortium [www.hybridmemorycube.org](http://www.hybridmemorycube.org)
- 3D-IC Alliance [www.3d-ic.org](http://www.3d-ic.org) (event & blogs/paper listing)

Discussion groups / 3D news:
- [www.3dincites.com](http://www.3dincites.com)
- [www.3d-ics.com](http://www.3d-ics.com)
- 3D-IC group on [www.linkedin.com](http://www.linkedin.com)